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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,843	11/12/2003	Altug Koker	10559-011003	9501

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/712,843	KOKER ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,2,5,7-11,15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weber (patent No. 4,959,779).

3. Weber taught the invention substantially as claimed including a data processing ("DP") system comprising (as per claims 1,8):

a) First circuit (28) receives addresses from a computer processor (CPU) and processes address information to determine a received data ordering of the data based on the data addresses (e.g., see figs. 1,2 and col. 4, line 32-col. 5, line 8)[the shift amount converter receives address data from the execution unit and determines the data ordering, converts the address data and sends address data signals to the load alignment and store alignment elements to indicate the ordering of the data; and

b) Second circuit (20,22) to reorder the data from the first circuit into ordered packets each in a predetermined ordering and to maintain information (e.g. see col. 4, line 16-col. 5, line 33)[data from the execution unit is reordered according the indication by the shift amount converter and address information is maintained in data order storage unit].

4. Weber did not expressly detail (claim 1,8) that the data was received by the first circuit in the implementation with CPU and all elements in fig. 1 on the same chip. However Weber taught an implementation with the CPU chip replaced by a chip set (e.g., see col. 3, lines 25-33). The in that implementation the CPU and the reordering elements would have been on different chips of the chipset. Therefore one of ordinary skill would have been motivated to send the data and address from the CPU to the Chip with the shift alignment converter at least to simplify the chipset implementation. Further since the data is not operated on by the first circuit then sending the data to the first circuit instead of directly to the second circuit that reorders the data does not change the operation of the claimed system and similarly would not have changed the operation of the Weber chipset.

5. As per claims 2,10 Weber taught a token generator (28) to receive and process the address information of the data to generate tokens corresponding to consecutive data packets, each token indicating at least the received data ordering and address of data in a respective packet (e.g., see fig. 1 and col. 4, line 32-col. 5, line 8).

6. As per claims 5,7,9 Weber taught the ordering to be linear corresponding to sequential addresses comprising four of the x86 orderings (e.g., see col. 5, lines 34-58) [little endian ,byte, half word, and big endian].

7. As per claim 11, Weber taught a separate data path(16) for the data and separate signal path for the tokens (e.g. see fig. 1).

8. As per claim 15, Weber taught a computer bus (18,24) connected to the chipset (e.g, see fig. 1 and col. 3, lines 25-33). As to a computer device connected to the computer bus one of ordinary skill would have motivated to connect any one of various standard computer devices such as memories input devices such a keyboard or mice or output devices such as modems , speakers , displays etc at least to provide the user or external computers the ability to interface with the computer system of Weber.

9. Claims 3,4,6,12-14,16,17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weber as applied to claims 1,2,5,7-11,15 above, and further in view of Childers (patent No. 5,634,013).

10. As per claim 3,12 Childers taught queue stage (511) having a token queue and a data queue (439,441,443) to respectively receive and store address tokens and the data, wherein queue are connected in a pipeline configuration with a first circuit and second circuit (457) (e.g., see figs. 3,4,5 and col. 7, lines 47-67).

11. As per claim 4,13 Weber taught a processing unit (453) to processing the tokens and data address information in the data queue and to generate control signals for reordering the data in each packet (e.g., see col. 8, lines 45-col. 9,line 22); a token buffer(511) to receive one token from the token queue; and a reordering unit(457) coupled to said processing unit and said token buffer and configured to reorder the data in each data packet in the predetermined ordering, the reordering unit forming a pipeline with the processing unit to begin processing a token for one data packet while reordering of a preceding data packet is completing (e.g., see figs. 3,4,5 and col. 7, lines 47-col. 8, line 46).

12. As per claim 6,14,16 Childers taught reordering for a graphics controller and to write and read plxel data regardless of format of agent such as video input device creates of expects to receive them. Therefore one of ordinary skill would have been motivated to take advantage of technology at the time of the of claimed invention and couple the system to a standard type of graphics controller namely a accelerated graphics port controller.

13. As per claim 17, Childers taught connection to a PCI bus to receive output from the system (e.g., see col. 3, lines 1-col. 4, line 44).

14. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Weber and Childers. Both references were directed to the conversion of the ordering of data in a data processing system. One of ordinary skill would have been motivated to incorporate the Childers teachings of queue to couple the reordering system to a graphics system at least to provide control of timing between the input and output and an further use of the system for reordering data for graphics applications.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Atallah (patent No. 5,519,842) disclosed a DP system for performing unaligned little endian and big endian data accesses in an processing system (e.g., see abstract).

Moyer (patent No. 5,907,865) disclosed a system for dynamically accessing both big endian and little endian storage schemes (e.g., se abstract).

Carnevale (patent No. 5,687,337) disclosed a mixed-endian computer system (e.g., see abstract).

Sethi (patent No. 6,370,633) disclosed a system for converting non-contiguous memory into contiguous memory for a graphics processor (e.g., see abstract).

Christie (patent No. 6,247,107) disclosed a chipset configured to perform data-directed prefetching (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER